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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,501	03/01/2004	Martin Vorbach	2885/85	1856

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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,501	VORBACH ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/946,810.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *030104*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file:

Preliminary Amendment dated 3/1/04

2. Claims 4-9 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 4-7 and 9 rejected under 35 U.S.C. 102(e) as being anticipated by Durham et al., U.S. Patent 6,785,826.

5. Regarding claim 4, Durham teaches a data processing device, comprising:

a. an array of data processing unit (functional units 206, 210, 214 and 218, figure 2), the processing unit being connected to at least on one of a power supply line and a clock line (system clock 800 via unit clock 804, figure 8; system clock 800 via unit clock 904); and

b. an enabling/disabling element configured (low power mode circuits of each functional unit include AND gates 802 figure 8; or MUXes 902, figure 9) to at least one of:

i. enable or disable power supply to a number of the processing units, and

ii. block full clock speed for the number of data processing units (the clock is either stopped or reduced for a particular functional unit, col. 7, line 34 through col. 8, line 7);

iii. wherein the number is less than all of the processing units (each functional unit controls its own power dissipation, col. 3, lines 44-48).

6. Regarding claim 5, Durham taught the data processing device according to claim 4, as described above. Durham further teaches wherein the enabling/disabling element is adapted to provide a clock to a number of the data processing units which is equal to 0 (Durham inherently teaches that clocks all data processing units may be stopped, col. 3, lines 44-48).

7. Regarding claim 6, Durham taught the data processing device according to claim 4, as described above. Durham further teaches wherein the enabling/disabling is adapted to be handshake-driven (Durham uses Request lines 208, 214, 220 and 228 along with Status lines 210, 216, 222 and 228 to communicate status and requests which are interpreted to be handshake-driven).

8. Regarding claim 7, Durham taught the data processing device according to claim 4, as described above. Durham further teaches wherein each of the processing units is a reconfigurable unit of a multi-dimensional array (each functional unit of Durham is reconfigurable because it can change its operating mode, col. 3, lines 44-48).

9. Regarding claim 9, Durham taught the data processing device according to claim 4, as described above. Durham further teaches wherein the enabling/disabling element is configured to selectively block full clock speed for the number of data processing units (each functional unit of Durham has clock control, col. 3, lines 44-48, figures 8 and 9).

10. Claim 4, 5, 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Gupta et al., U.S. Patent 5,996,083.

11. Regarding claim 4, Gupta teaches a data processing device comprising:

a. an array of data processing units (FU_1-FU_2, figure 2), the data processing units being connected to at least one of a power supply line (removing power to functional unit, col. 4, lines 5-7; figure 6 and corresponding text) and a clock line (col. 3, line 67 through col. 4, line 5; figures 3-5 and corresponding text); and

b. an enabling/disabling element configured (power control 108, figure 2) to at least one of:

i. enable or disable power supply to a number of the processing units (removing power to the functional units, col. 4, lines 5-7), and

ii. block full clock speed for the number of data processing units (col. 3, line 67 through col. 4, line 5);

iii. wherein the number is less than all of the processing units (each functional may be provided with it own clock and power control col. 3, lines 47-51; figures 3-6 and corresponding text).

12. Regarding claim 5, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein the enabling/disabling element is adapted to provide a clock to a number of the data processing units which is equal to 0 (all or none of the processing units of Gupta may be enabled or disabled, col. 3, lines 47-51; figures 3-5 and corresponding text).

13. Regarding claim 7, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein each of the processing units is a reconfigurable unit of a multi-dimensional array (each processing unit of Gupta is reconfigurable because it can change its operating mode, col. 3, line 64 through col. 4, line 5).

14. Regarding claim 8, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein the enabling disabling element is configured to selectively enable or disable power supply to the number of data processing units (figure 6 and corresponding text).

15. Regarding claim 9, Gupta taught the data processing device according to claim 4, as described above. Gupta further teaches wherein the enabling/disabling element is configured to selectively block full clock speed for the number of data processing units (figures 3-5 and corresponding text).

16. Claim 4, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Hansen et al., U.S. Patent 4,498,134.

17. Regarding claim 4, Hansen teaches a data processing device comprising:

a. an array of data processing units (segregatable Array Processor 61), the data processing units being connected to at least one of a power supply line (col. 34, lines 48-63) and a clock line; and

b. an enabling/disabling element configured (the Segregator Functional Plane, col. 34, lines 48-63) to at least one of :

i. enable or disable power supply to a number of the processing units (electrically sever connection to unused or inactive functional planes to reduce power of the array processor, col. 34, lines 48-63), and

ii. block full clock speed for the number of data processing units;

c. wherein the number is less than all of the processing units (only unused planes are disabled, col. 34, lines 48-63).

18. Regarding claim 7, Hansen taught the data processing device according to claim 4, as described above. Hansen further teaches wherein each of the processing units is a reconfigurable unit of a multi-dimensional array (each processing unit of Hansen is reconfigurable because it can change its operating mode and each is part of an array of processors 61 comprised of processors 60, figure 1, col. 5, lines 40-49, and col. 34, lines 23-63).

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (8:00 am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James K. Trujillo
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Technology Center 2100